



emulation and clock and synchronization and l

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KY Yun, AE Dooply - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1999

- [ieeexplore.ieee.org](#)

... by the sampling **latch** at the module boundary. In our scheme, the **synchronization** failure is circumvented by pausing or stretching the local module **clock** when ...

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[Synchronous handshake circuits - group of 6 »](#)

A Peeters, K van Berkel - Proc. International Symposium on Advanced Research in ... - [doi.ieeecomputersociety.org](#)

... Only this time, the updates of the state variable \bar{U} take place upon rising edges of the **clock**, and the state is stored in a **flip-flop** rather than a **latch**. ...

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[Serial Fault Emulation - group of 8 »](#)

L Burgun, F Reblewski, G Fenelon, J Barbier, O ... - Proc. DAC - [doi.ieeecomputersociety.org](#)

... FPGA reconfiguration so that only one **emulation** run will ... edge-triggered **flip-flop** or a **latch** and it ... devices are synchronized by a complex **clock** system ensuring ...

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[\[book\] Boundary-Scan Test: A Practical Approach](#)

H Bleeker, V Den Eijnden, F de Jong - 1993 - [books.google.com](#)

... **Clock IDI Clock** TO Page 23. Fig. 1-12 ShiftDR state PCB Testing 9Notice that in figure 1-12 the Boundary-Scan design comprises, a parallel **latch (flip-flop)** and ...

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[Static scheduling of multidomain circuits for fast functional verification - group of 3 »](#)

M Kudlugi, R Tessier - Computer-Aided Design of Integrated Circuits and Systems, ..., 2002 - [ieeexplore.ieee.org](#)

... paper presents new scheduling and **synchronization** techniques to ... asynchronous **clock** domains in logic **emulation** systems is ... **flip-flop** whose gate/clock input is ...

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[Replace Your Am7968 TAXI™ Transmitter With a CY7B923 HOTLink™ - group of 5 »](#)

A Functionality - [eetkorea.com](#)

... sixteen patterns are used to define **synchronization** and in ... the falling edge of the reference **clock** where data ... **HOTLink Emulation** of Am7968 To create a drop-in ...

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[Design verification of complex microprocessors - group of 3 »](#)

J Yim, C Park, W Yang, H Oh, H Choi, S Lee, N Won, ... - Circuits and Systems, 1996.. IEEE Asia Pacific Conference on, 1996 - [ieeexplore.ieee.org](#)

... The cost of **emulation** hardware is very high and re ... to provide a buffer- ing and **synchronization** mechanism between ... pipeline 55,415 Verilog HDL **Clock** and event ...

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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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clock tree

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Zero skew clock routing with minimum wirelength.

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TH Chao, YC Hsu, JM Ho, KD Boese, AB Kahng - IEEE Transactions on Circuits and Systems II: Analog and ..., 1992 - csa.com

... In this paper, we first present the deferred-merge embedding (DME) algorithm, which embeds any given connection topology to create a clock tree with zero skew ...

Cited by 111 - [Web Search](#)

Activity-driven clock design for low power circuits - group of 2 »

GE Téllez, A Farrahi, M Sarrafzadeh - Proceedings of the 1995 IEEE/ACM international conference on ..., 1995 - portal.acm.org

... Activity-Driven Clock Tree Construction Problem (ADCTC): Let the activity pattern of a clock tree node be obtained by ORing the patterns of its sinks. ...

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Skew sensitivity minimization of buffered clock tree - group of 6 »

J Chung, CK Cheng - Proceedings of the 1994 IEEE/ACM international conference on ..., 1994 - portal.acm.org

Abstract Given a topology of clock tree and a library of buffers, we propose an efficient skew sensitivity minimization algorithm using dynamic programming ...

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UST/DME: A Clock Tree Router For General Skew Constraints - group of 13 »

CWENA TSAO, CKOK KOH - portal.acm.org

Page 1. UST/DME: A Clock Tree Router For General ... [1996], and Neves and Friedman [1996] belong to the first category of research on clock tree synthesis. ...

Cited by 27 - [Web Search](#) - [BL Direct](#)

Clock routing for high-performance ICs - group of 2 »

MAB Jackson, A Srinivasan, ES Kuh - Design Automation Conference, 1990. Proceedings. 27th ACM/ ..., 1990 - ieeeexplore.ieee.org

... To understand the consequences of decisions made during physical design, one must model the interconnect parasitics that load the clock tree. ...

Cited by 102 - [Web Search](#)

Power optimal buffered clock tree design - group of 6 »

A Vittal, M Marek-Sadowska - Proceedings of the 32nd ACM/IEEE conference on Design ..., 1995 - portal.acm.org

... A bounded skew clock tree is synthesized and power reduction is achieved by reducing the wire length; this is not power optimal as the power dissipated by the ...

Cited by 21 - [Web Search](#) - [BL Direct](#)

Zero skew clock net routing - group of 3 »

TH Chao, YC Hsu, JM Ho, HC ITRI - Design Automation Conference, 1992. Proceedings., 29th ACM/ ..., 1992 - ieeeexplore.ieee.org

... routes from the center of the set into the centers of the two subsets, and ensures an exact balance and no length skew at the current level of the clock tree. ...

Cited by 83 - [Web Search](#)

Zero-skew clock routing trees with minimum wirelength

KD Boese, AB Kahng - ASIC Conference and Exhibit, 1992., Proceedings of Fifth ..., 1992 - ieeeexplore.ieee.org



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Verifying Synchronization in Multi-Clock Domain SoC - group of 2 » [All articles](#) [Recent articles](#)

T Kapschitz, R Ginosar, R Newton - 2004 - cs.huji.ac.il

... The most commonly used **synchronizer** is based ... or combinational logic driving **flip-flop**- based synchronizers ... typically starts with the **clock tree** being identified ...

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A new synchronizer design - group of 3 »

J Walker, A Cantoni - Computers, IEEE Transactions on, 1996 - ieeeexplore.ieee.org

... Tzeng and HL Chen, "Structural and **Tree** Embedding Aspects ... region of time associated with each **clock** event such ... considered to occur when the **flip-flop** at the ...

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A Survey of Clocking Strategies from Synchronous to Asynchronous

M Heath - www-unix.ecs.umass.edu

... as the response properties of a **flip-flop** from a ... 6. Stoppable Clocks – The Alternative to the **Synchronizer** ... oscillator at the root of the **clock tree** is not ...

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Asynchronous & Synchronous Reset Design Techniques-Part Deux - group of 5 »

CE Cummings, D Mills, S Golsen - SNUG Boston 2003 - sunburst-design.com

... the reset can occur within one **clock** period ... timing analysis for a reset **tree** must be ... design uses the distributed reset **synchronizer flip-flop tree** discussed in ...

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CLOCK DOMAIN CROSSING - group of 2 »

R Biddappa - cadence.co.in

... Figure 4: Two **flip-flop synchronizer** solution ... may specify a two-flop **synchronizer** from CLK 3 ... partition and topology checks – Proper **clock tree** definition and ...

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Low Latency Synchronization Through Speculation

E Macii... - Springer

... performance sys- tems using IP blocks with large **clock trees** [2]. Figures of ... Write **Clock** ... In the speculative **synchronizer** the first **flip-flop** must be tested to ...

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Clock signals

SC Specifications - ee.byu.edu

... Input is sampled at this **clock** edge. Input: Value sampled by **flip-flop** at **clock** edge. Example: D **Flip-Flop** Input **Clock** Output BYU ECEn 493R ...

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Design of On-chip and Off-chip Interfaces for a GALS NoC Architecture

E Beigné, P Vivet - doi.ieeecomputersociety.org

... fifo is not strictly required : a simple 2 **flip-flop synchronizer** could be ... write_enable1 write_clk write_clock (leaf cells) **Clock-Tree** write_enable0 E_ACCEPT1a ...

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 Dragone, S.; Lombriser, C.;
[Rapid System Prototyping, 2005. \(RSP 2005\). The 16th IEEE International Wo](#)
 8-10 June 2005 Page(s):211 - 217
 Digital Object Identifier 10.1109/RSP.2005.51
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 Nose, K.; Shibayama, A.; Kodama, H.; Mizuno, M.; Edahiro, M.; Nishi, N.;
[Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC, 200](#)
 International
 6-10 Feb. 2005 Page(s):296 - 599 Vol. 1
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[Design Automation Conference, 2005. Proceedings. 42nd](#)
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 Dobkin, R.; Ginosar, R.; Sotiriou, C.P.;
[Asynchronous Circuits and Systems, 2004. Proceedings, 10th International Sy](#)
 19-23 April 2004 Page(s):170 - 179
 Digital Object Identifier 10.1109/ASYNC.2004.1299298
[AbstractPlus](#) | Full Text: [PDF](#)(1408 KB) IEEE CNF
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- ☐ **5. Communication analysis for system-on-chip design**
 Siebenborn, A.; Bringmann, O.; Rosenstiel, W.;
[Design Automation and Test in Europe Conference and Exhibition, 2004. Proc](#)
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1 [Static scheduling of multiple asynchronous domains for functional verification](#)



Murali Kudlugi, Charles Selvidge, Russell Tessier

 June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(99.70 KB)

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While ASIC devices of a decade ago primarily contained synchronous circuitry triggered with a single clock, many contemporary architectures require multiple clocks that operate asynchronously to each other. This multi-clock domain behavior presents significant functional verification challenges for large parallel verification systems such as distributed parallel simulators and logic emulators. In particular, multiple asynchronous design clocks make it difficult to verify that design hold ...

2 [Serial fault emulation](#)



Luc Burgun, Frédéric Reblewski, Gérard Fenelon, Jean Barbier, Olivier Lepape

 June 1996 **Proceedings of the 33rd annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(105.22 KB)

 Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Session 1A: Dynamic verification: Static scheduling of multi-domain memories for functional verification](#)

Murali Kudlugi, Charles Selvidge, Russell Tessier

 November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(113.07 KB)

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Over the past decade both the quantity and complexity of available on-chip memory resources have increased dramatically. In order to ensure accurate ASIC behavior, both logic functions and memory resources must be successfully verified before fabrication. Often, the functional verification of contemporary ASIC memory is complicated by the presence of multiple design clocks that operate asynchronously to each other. The presence of multiple clock domains presents significant challenges for large ...



asynchronous + synchronous + synchronizer

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D Peleg, JD Ullman - Proceedings of the sixth annual ACM Symposium on Principles ... 1987 - portal.acm.org

... 3. Synchronizers The **synchronizer** is intended to enable any **synchronous** algorithm to run on any **asynchronous** network. The goal of ...

Cited by 125 - [Web Search](#)

[Practical Design of Globally-Asynchronous Locally-Synchronous Systems - group of 7 »](#)

J Mutersbach, T Villiger, W Fichtner - ... on Advanced Research in Asynchronous Circuits and Systems (... , 2000 - doi.ieeecomputersociety.org

... scheme does not impair performance with **synchronizer's** latency. ... consumption in clock by using globally **asynchronous**, locally **synchronous** design style ...

Cited by 72 - [Web Search](#)

[Performance of synchronous and asynchronous schemes for VLSI systems - group of 6 »](#)

M Afghahi, C Svensson - IEEE Transactions on Computers, 1992 - doi.ieeeecs.org

... acceptable for scaled-down **synchronous** VLSI systems. A module in an **asynchronous** system, Fig. 1(b), may be represented by an input **synchronizer** (FF) and the ...

Cited by 53 - [Web Search](#)

[Interfacing synchronous and asynchronous modules within a high-speed pipeline - group of 13 »](#)

AE Sjogren, CJ Myers - Very Large Scale Integration (VLSI) Systems, IEEE ... , 2000 - ieeeexplore.ieee.org

... Pipeline syn-chronization extends the double-latching idea by inserting more pipeline latches between the **asynchronous** and **synchronous** module [10]. While each ...

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[Globally-asynchronous locally-synchronous architectures to simplify the design of on-chip systems - group of 3 »](#)

J Mutersbach, T Villiger, H Kaeslin, N Felber, W ... - ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE ... , 1999 - ieeeexplore.ieee.org

Page 1. Globally-Asynchronous Locally-Synchronous Architectures to Simplify the Design of On-Chip Systems Jens Mutersbach, Thomas ...

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[Unifying synchronous and asynchronous message-passing models - group of 11 »](#)

M Herlihy, S Rajsbaum, MR Tuttle - Proceedings of the seventeenth annual ACM symposium on ... , 1998 - portal.acm.org

... passing model when he constructed his **synchronizer** and showed how (in the absence of faults) **synchronous** protocols can be run in **asynchronous** systems in the ...

Cited by 24 - [Web Search](#)

[Montage: An fpga for synchronous and asynchronous circuits - group of 6 »](#)

S Hauck, G Borriello, S Burns, C Ebeling - 2nd International Workshop on Field-Programmable Gate Arrays ... , 1992 - ee.washington.edu

... For **synchronous** circuit elements, this line carries the ... stateholding function such as an **asynchronous** SR flipflop ... enabled arbiter, or a **synchronizer**, with all ...

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